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Sheet 1 of 1

Form 1449

Atty. Docket No.: 499.028US1

Group 2700
Serial No. 09476,678INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(Use several sheets if necessary)

Applicant: Philip Nord Jenkins et al.

Filing Date: December 30, 1999

Group: Unknown

U. S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
gm	4,514,749	04/30/1985	Shoji, M.	357	68	01/18/83
gm	4,587,445	05/06/1986	Kanuma, A.	307	443	05/16/84
gm	4,926,066	05/15/1990	Maini, R., et al.	307	303	09/12/88
gm	5,295,132	03/15/1994	Hashimoto, K., et al.	370	13	08/25/92
gm	5,315,175	05/24/1994	Langner, P.A.	307	443	03/18/93
gm	5,416,606	05/16/1995	Katayama, A., et al.	358	467	09/23/94
gm	5,481,567	01/02/1996	Betts, W.L., et al.	375	261	09/12/94
gm	5,604,450	02/18/1997	Borkar, S., et al.	326	82	07/27/95
gm	5,657,346	08/12/1997	Lordi, A.L., et al.	375	224	10/13/95
gm	5,793,259	08/11/1998	Chengson, D.	331	78	06/20/97
gm	5,811,997	09/22/1998	Chengson, D.P., et al.	327	112	04/26/96
gm	5,847,592	12/08/1998	Gleim, G., et al.	327	403	09/13/94
gm	5,898,729	04/27/1999	Boezen, H., et al.	375	259	10/10/95

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OTHER DOCUMENTS

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gm	"Low Power Quad Differential Line Driver with Cut-Off", <u>National Semiconductor, F100K ECL 300 Series Databook and Design Guide, pp. 2-54 - 2-60, (1992)</u>
gm	Djordjevic, A.R., et al., "Time Domain Response of Multiconductor Transmission Lines", <u>Proceedings of the IEEE, 75(6), 743-64, (June 1987)</u>
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gm	Takahashi, T., et al., "110GB/s Simultaneous Bi-Directional Transceiver Logic Synchronized with a System Clock", <u>IEEE International Solid-State Circuits Conference, 176-177, (1999)</u>

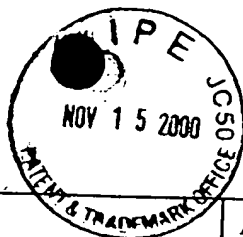
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Sheet 1 of

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Applicant: Philip Nord Jenkins et al.

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Group: 2816

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Gm	4,477,713	10/16/1984	Cook, G.E., et al.	219	124.34	07/09/82
GM	4,823,184	04/18/1989	Belmares-Sarabia, et al.	358	27	09/08/87
Gm	5,544,203	08/06/1996	Casasanta, J.A., et al.	375	376	10/18/94
GM	5,844,954	12/01/1998	Casasanta, J.A., et al.	375	373	02/20/97
GM	6,005,895	12/21/1999	Perino, D.V., et al.	375	288	12/20/96

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Gm	"The SA27 library includes programmable delay elements DELAYMUXO and DELAYMUXN. How are these cells used?", IBM Delaymuxn Book, pp. 1-6, (February 1999)					
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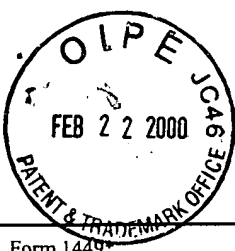
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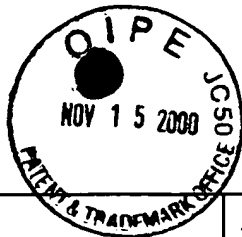
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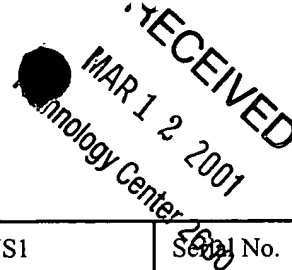
William M. ...

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Gm	5,583,454	12/10/1996	Hawkins, K.G., et al.	326	81	12/01/95
Gm	5,790,838	08/04/1998	Irish, J.D., et al.	395	555	08/20/96
Gm	5,802,103	09/01/1998	Jeong, K.	375	220	12/29/95
Gm	5,872,471	02/16/1999	Ishibashi, K., et al.	327	98	12/24/96
Gm	5,920,213	07/06/1999	Graf, III, W.A.	327	144	03/28/97
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Gm	Lee, K., et al., "A CMOS Serial Link for 1 Gbaud Fully Duplexed Data Communication", Symposium on VLSI Circuits, US, NY IEEE, XP000501054, 125-126, (June 9, 1994)

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<u>GM</u>	5,870,340	02/09/1999	Ohsawa, T.	365	189.02	07/08/97
<u>GM</u>	6,100,735	08/08/2000	Lu, C.Y.	327	158	11/19/98
<u>GM</u>	6,104,223	08/15/2000	Chapman, D.J., et al.	327	276	01/30/98

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